

**SECRET**

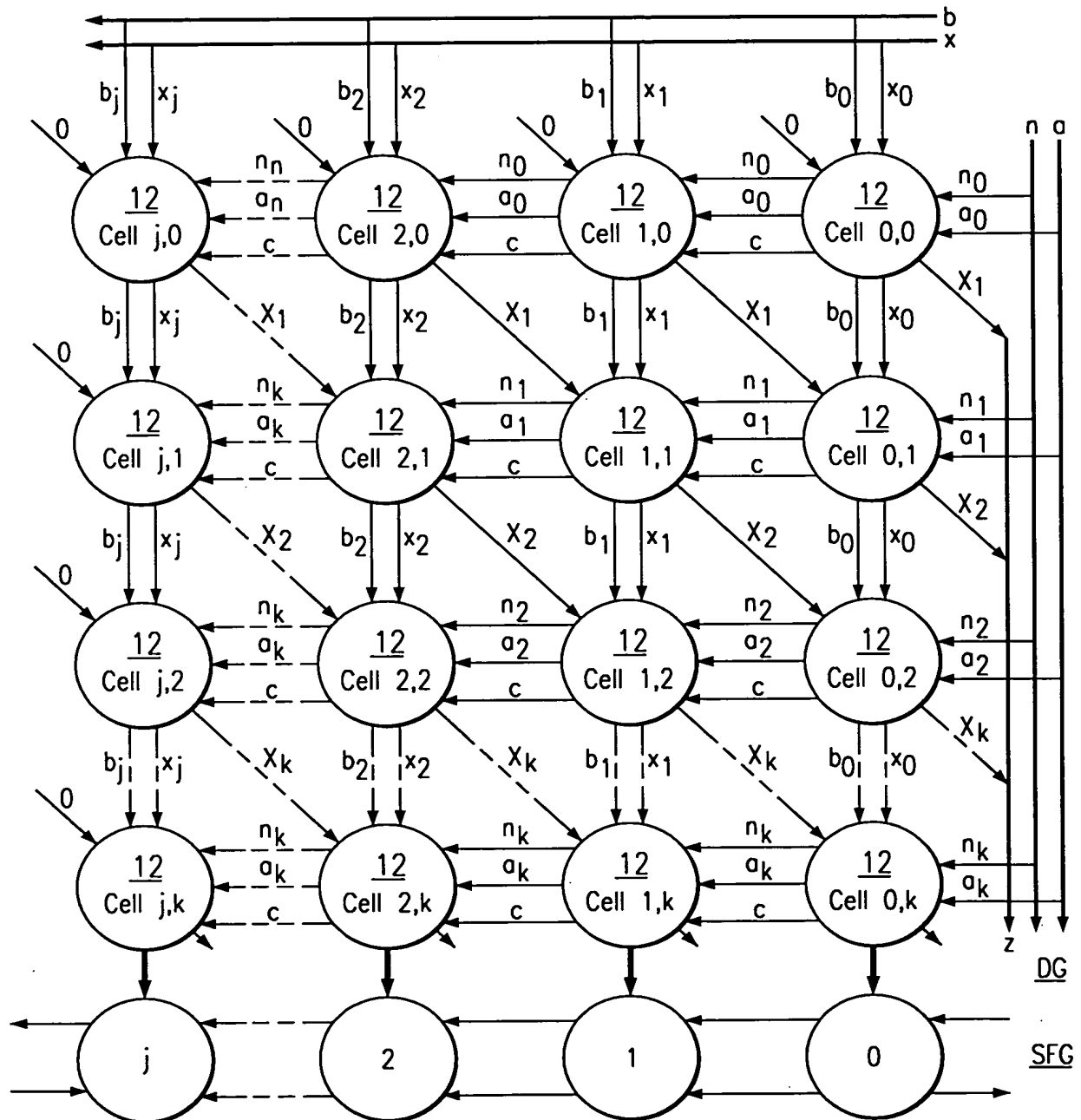


FIG. 2

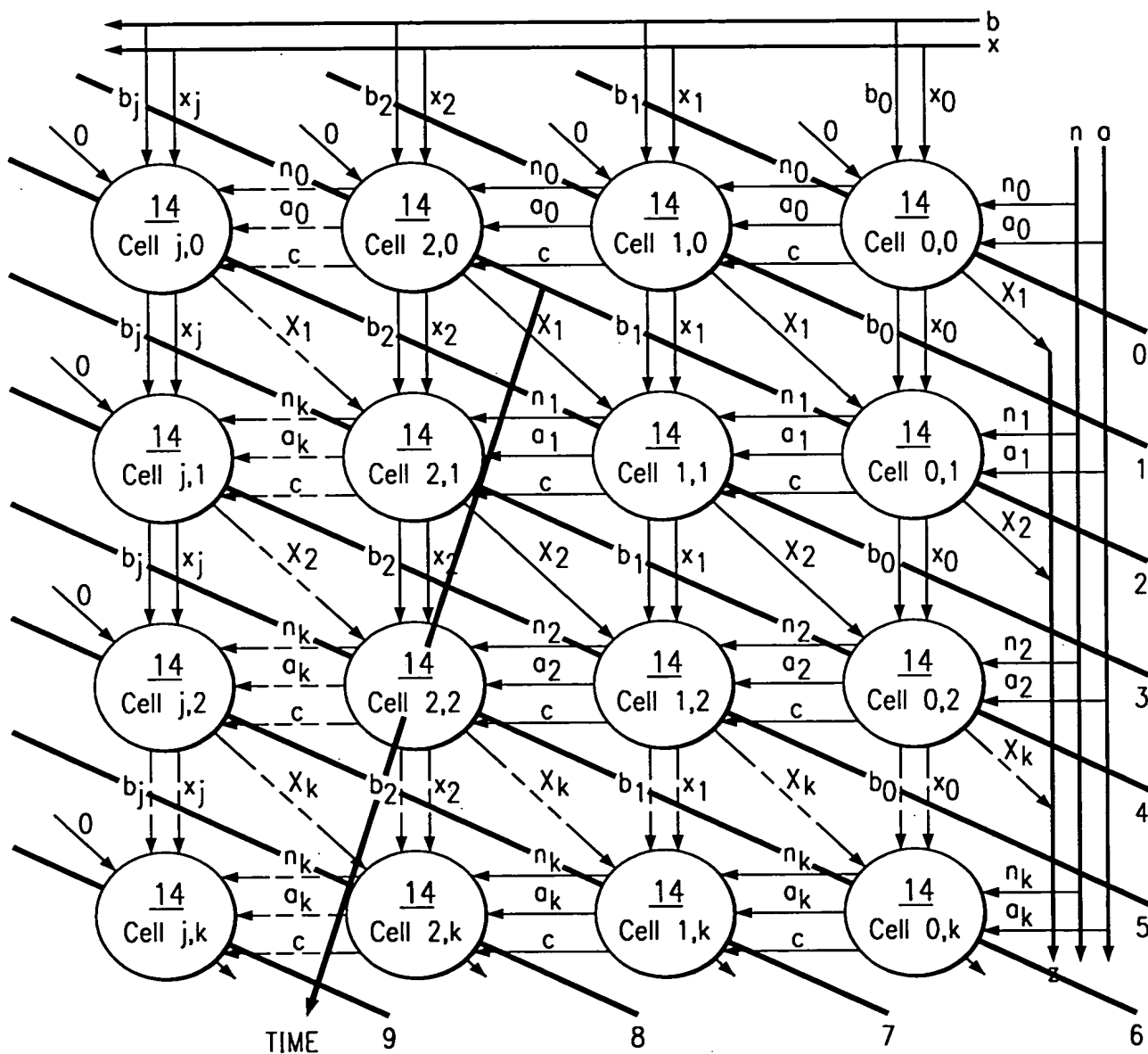


FIG. 3

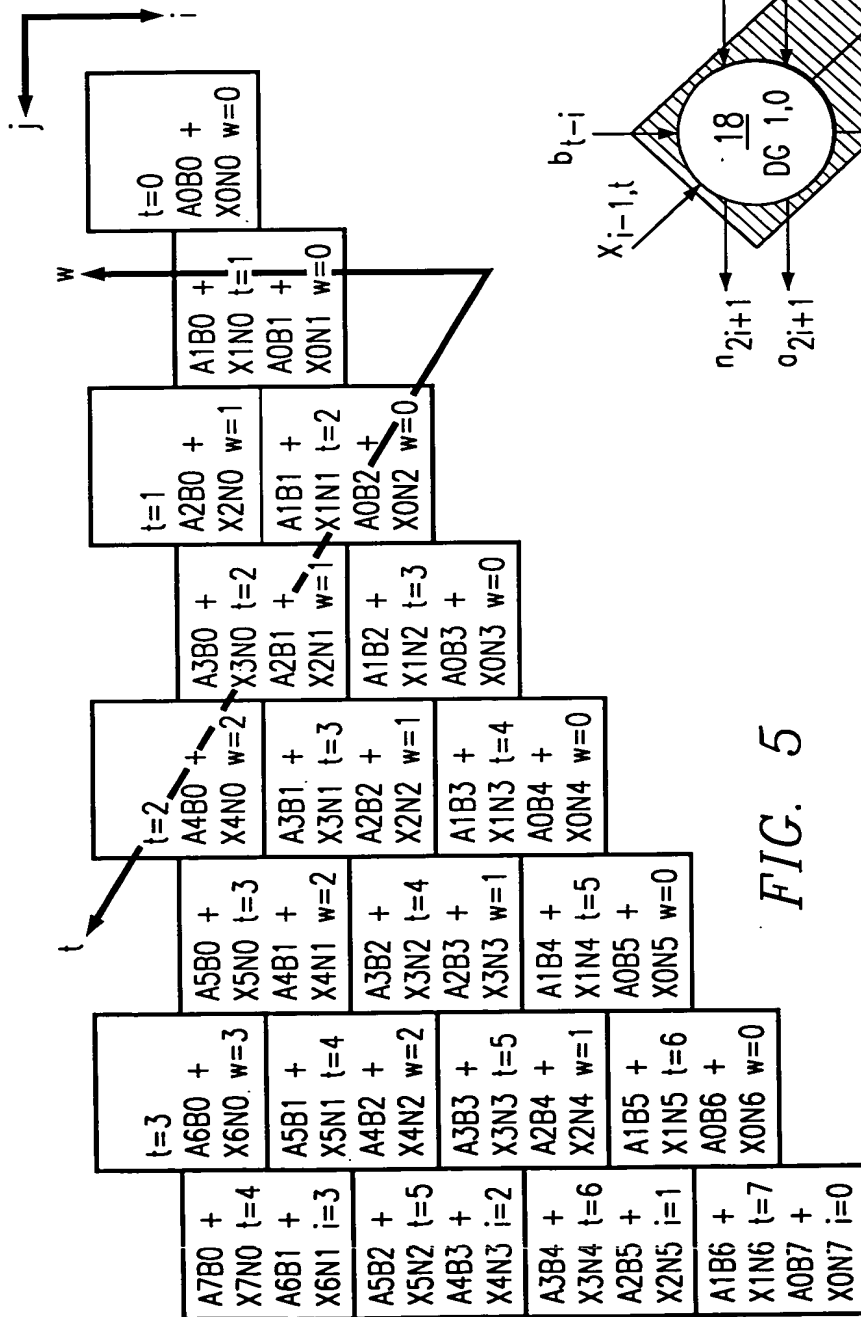


FIG. 5

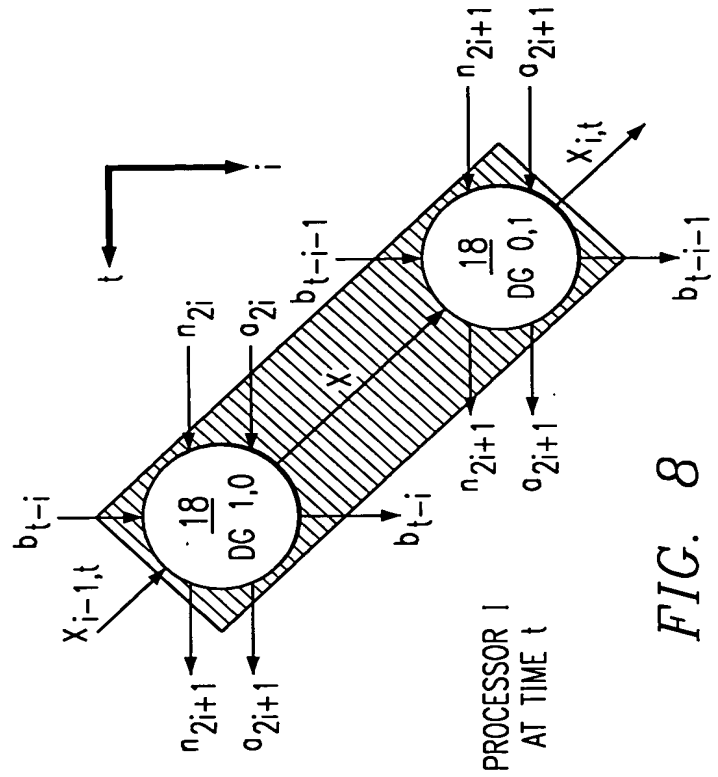


FIG. 8

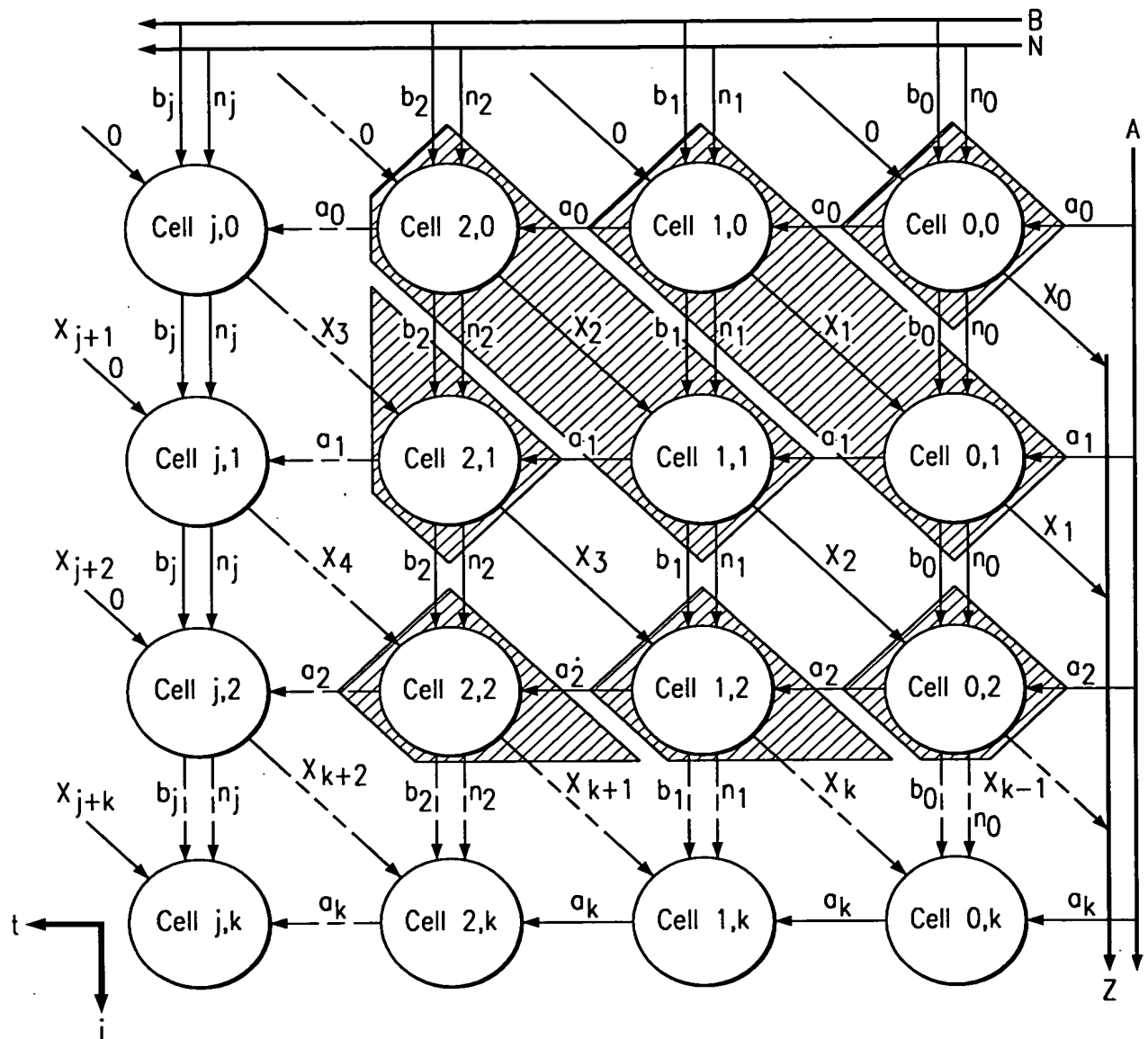


FIG. 6

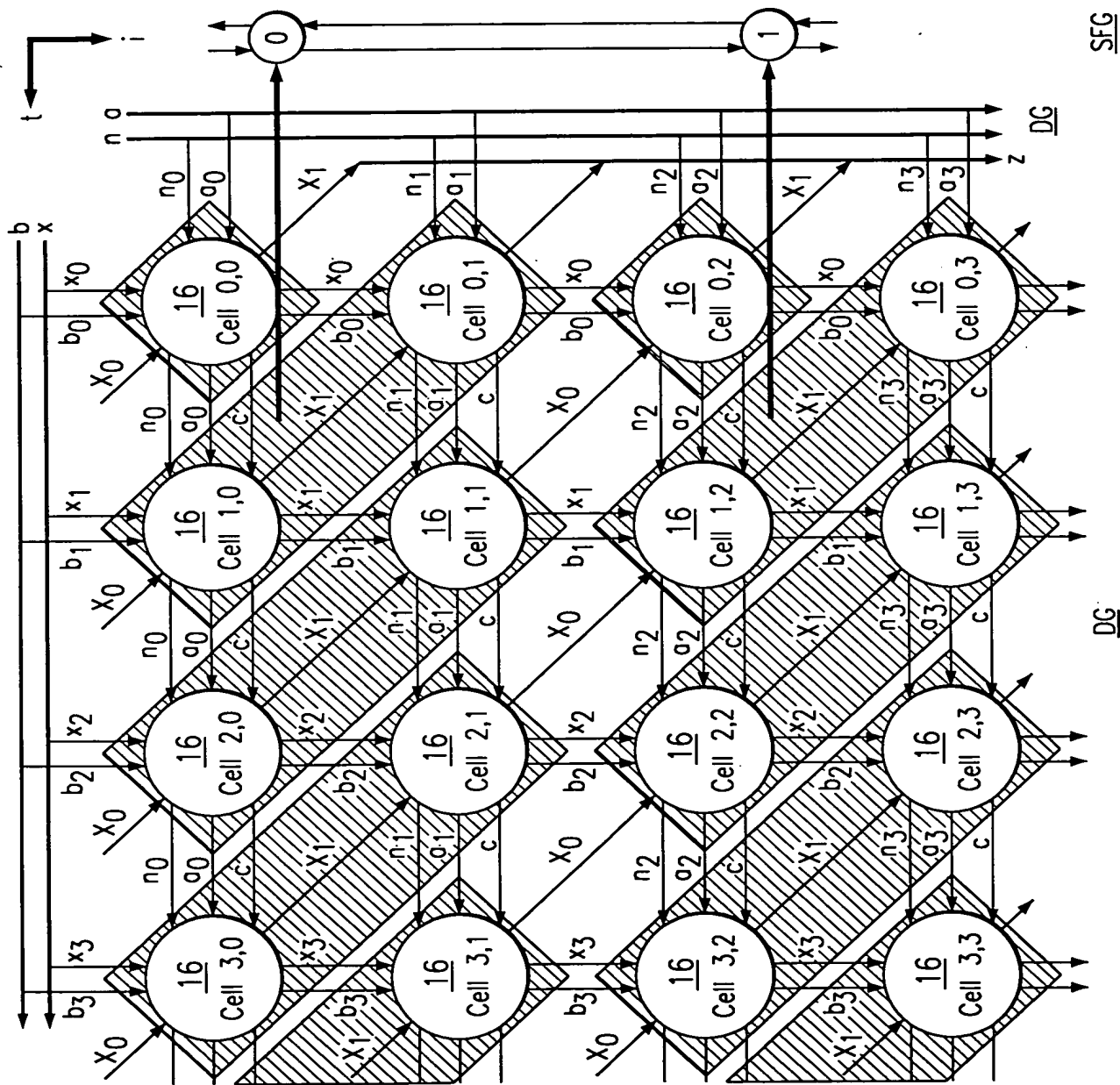


FIG. 7

SFG

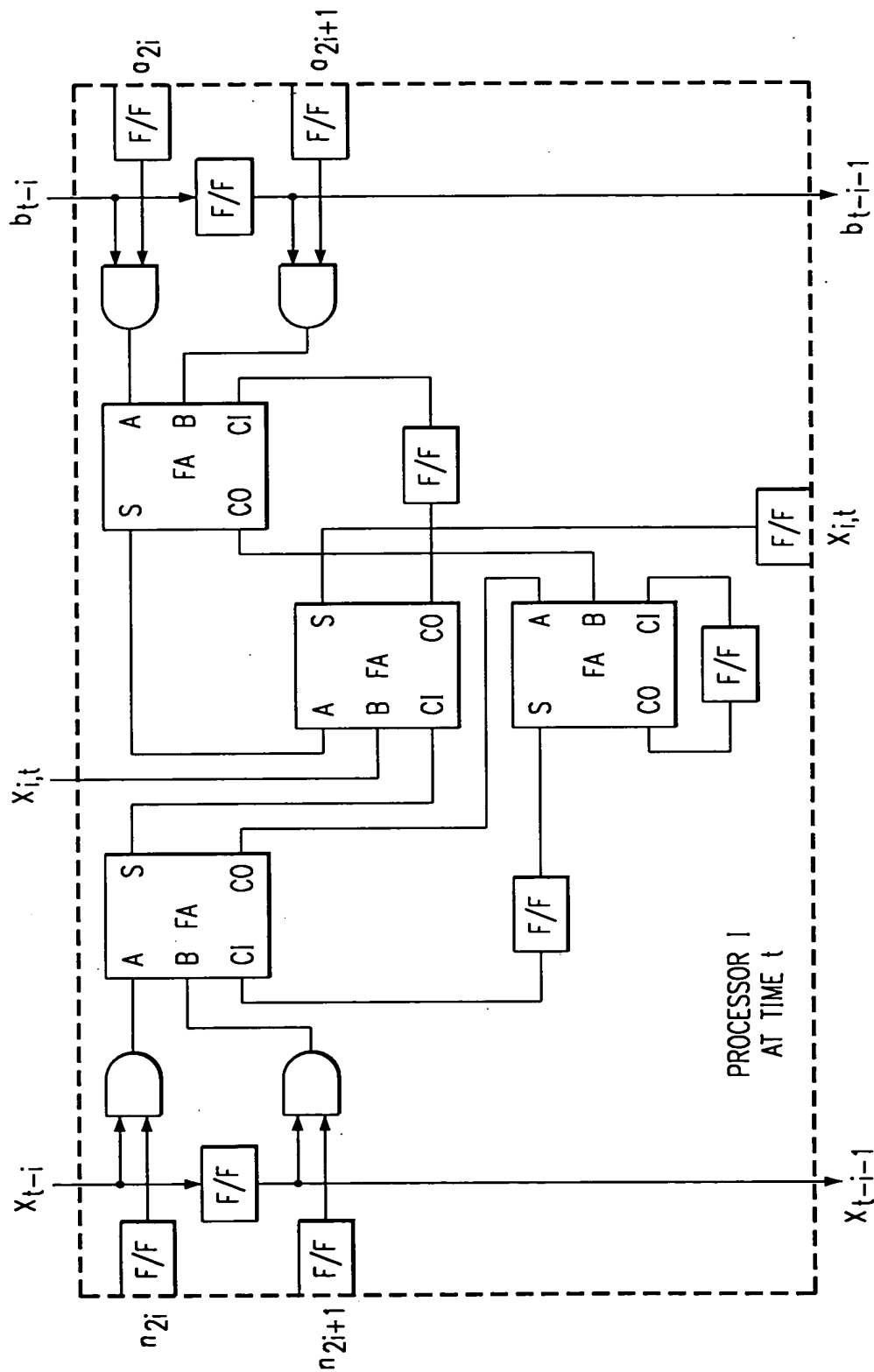


FIG. 9

Process TypicalBinaryMultiply (A,B)

```

Z:=0;
For i in 0 to n-1 loop
  c := 0;
  For j in 0 to n-1 loop
     $Z_{i+j} := (Z_{i+j} + A_i * B_j + c) \bmod 2$ ;
     $c := (Z_{i+j} + A_i * B_j + c) \div 2$ ;
  end loop;
  for j: in n to 2n-1 loop
     $Z_j := (Z_j + c) \bmod 2$ ;
     $c := (Z_j + c) \div 2$ ;
  end loop;
  transmit  $Z_i$ ;
end loop;

```

Process Reduce( $Z_i$ , N)

```

c := 0;
For i in 0 to n-1 loop
  wait for  $Z_i$ ;
   $X_i := Z_i$ ;
   $X_i := (X_i + x * N_i + c) \bmod 2$ ;
   $c := (X_i + x * N_i + c) \div 2$ ;
end loop;
X := X/2;
For i in 1 to k-1 loop
  x = X mod 2; c := 0;
  For j in 0 to n-1 loop
     $X_j := (X_j + x * N_j + c) \bmod 2$ ;
     $c := (X_j + x * N_j + c) \div 2$ ;
  end loop;
  X = X/2;
end loop;

```

BITS OF Z FEED  
SEQUENTIALLY  
ACROSS

FIG. 10

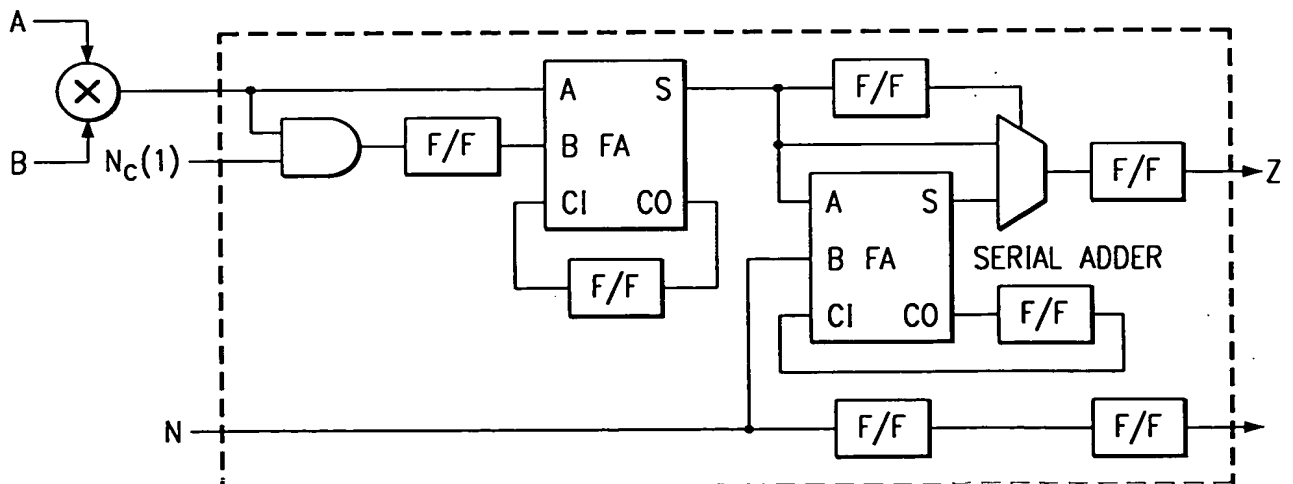


FIG. 18



064751.0315

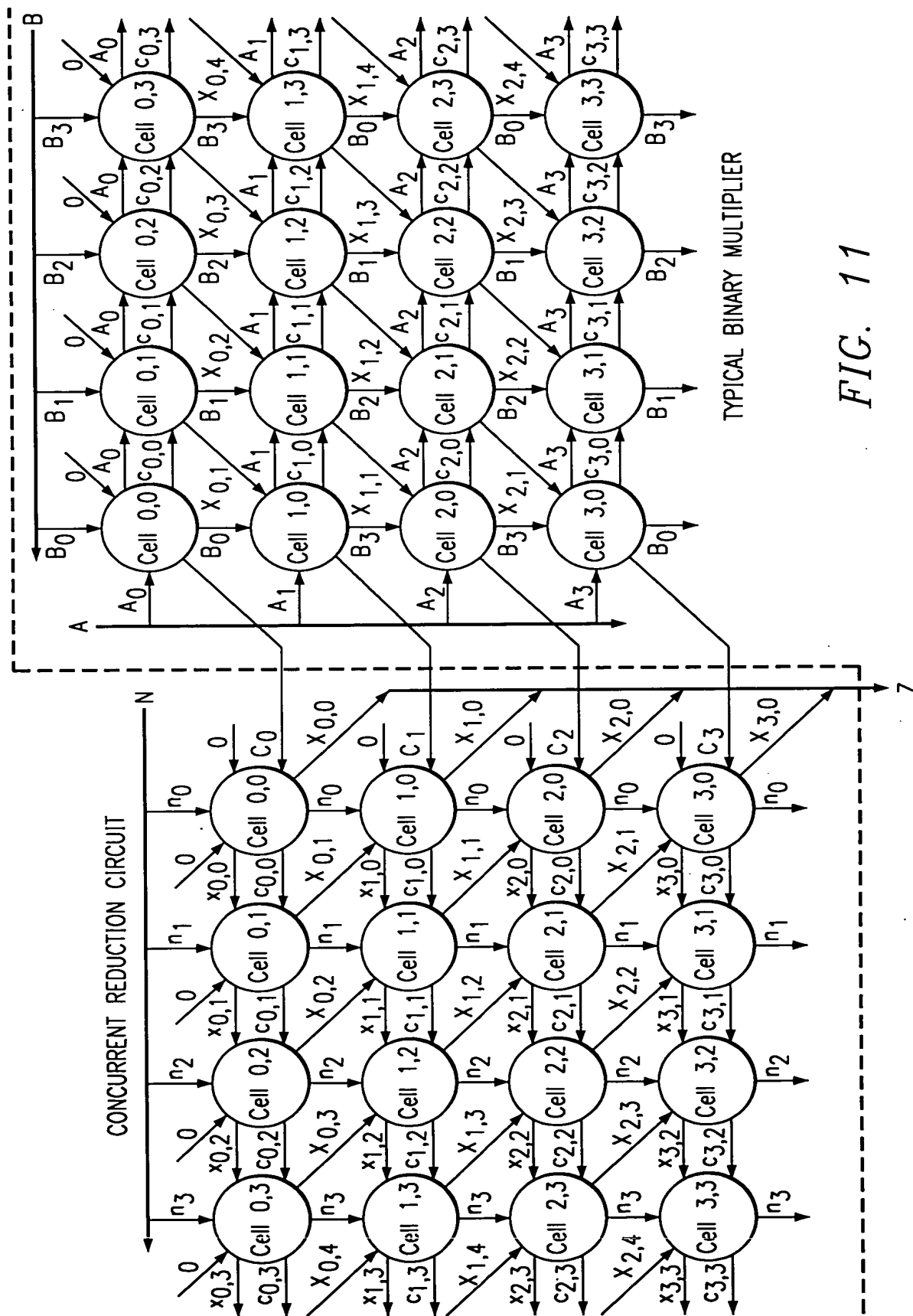


FIG. 11

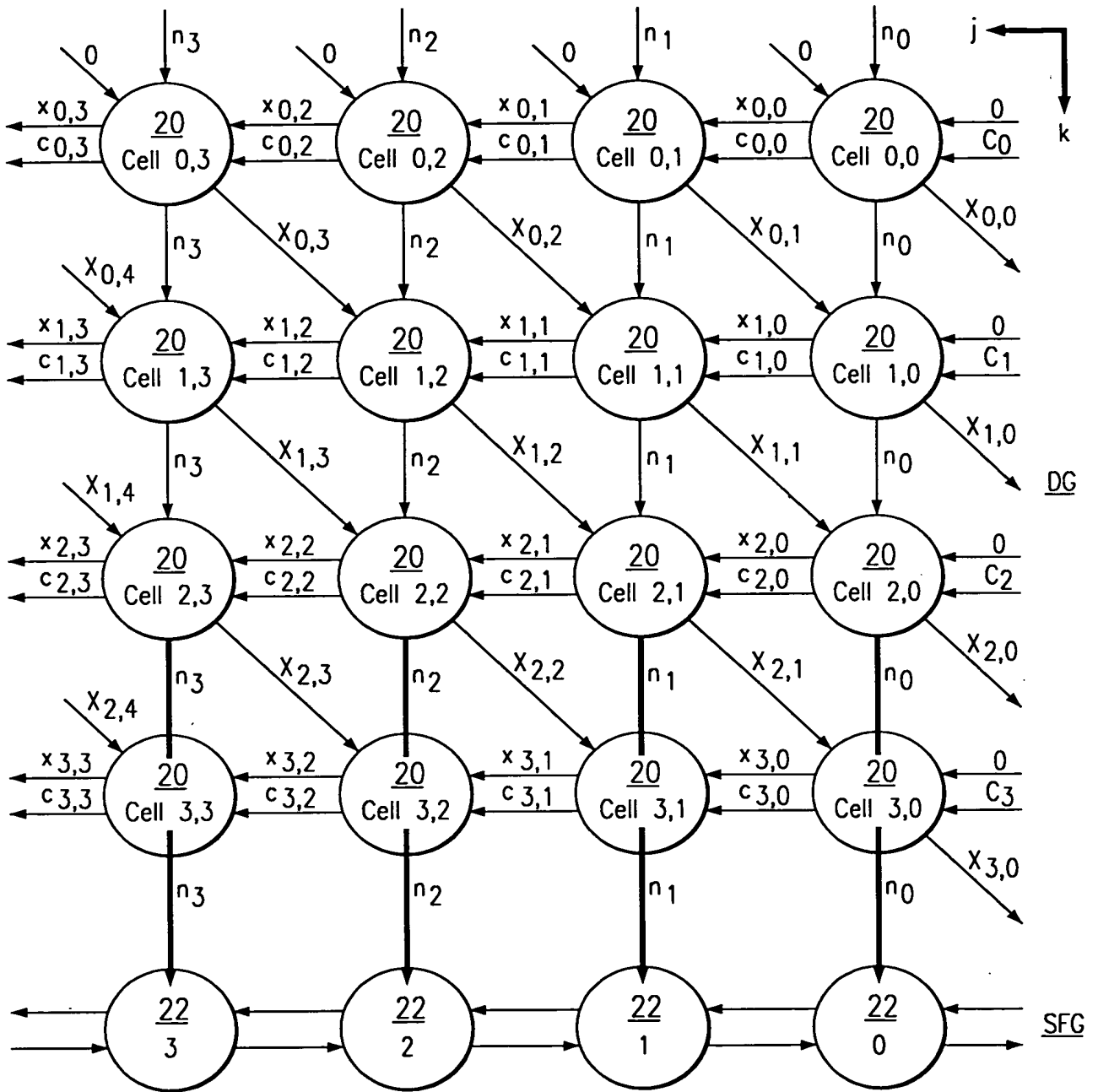


FIG. 12

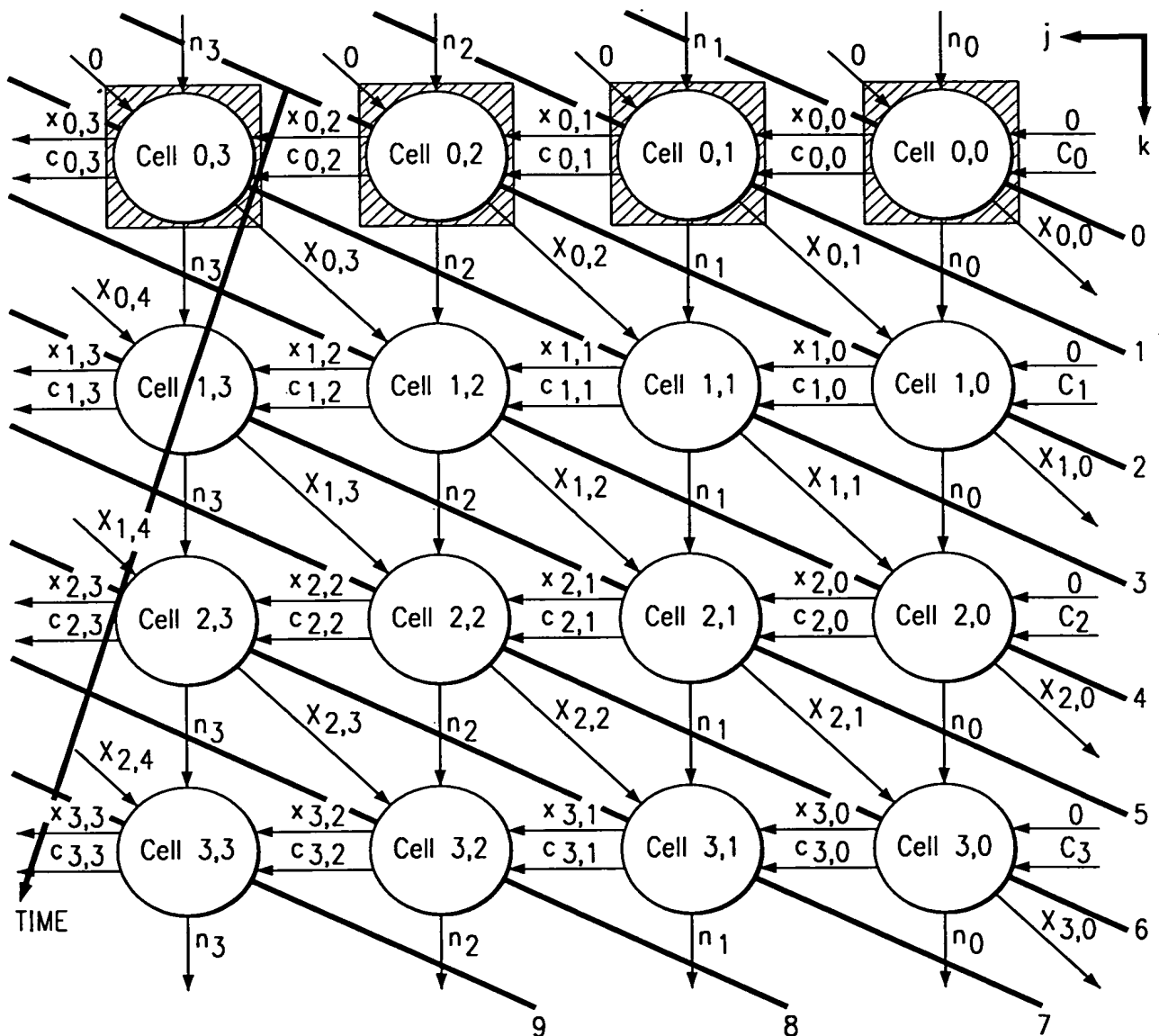


FIG. 13

FIG. 14

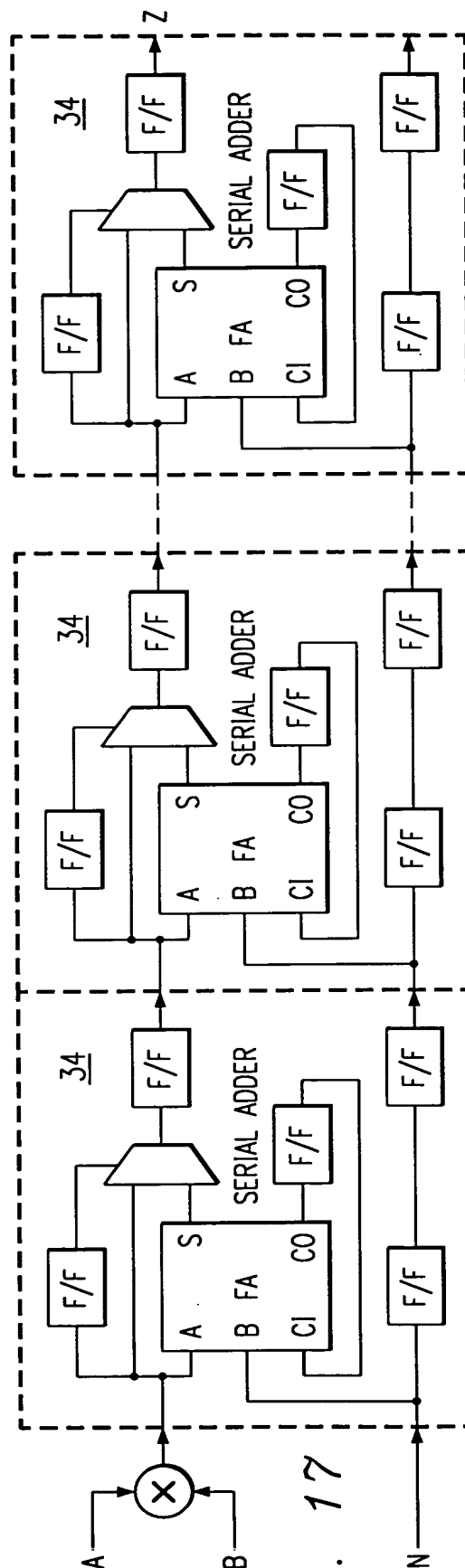
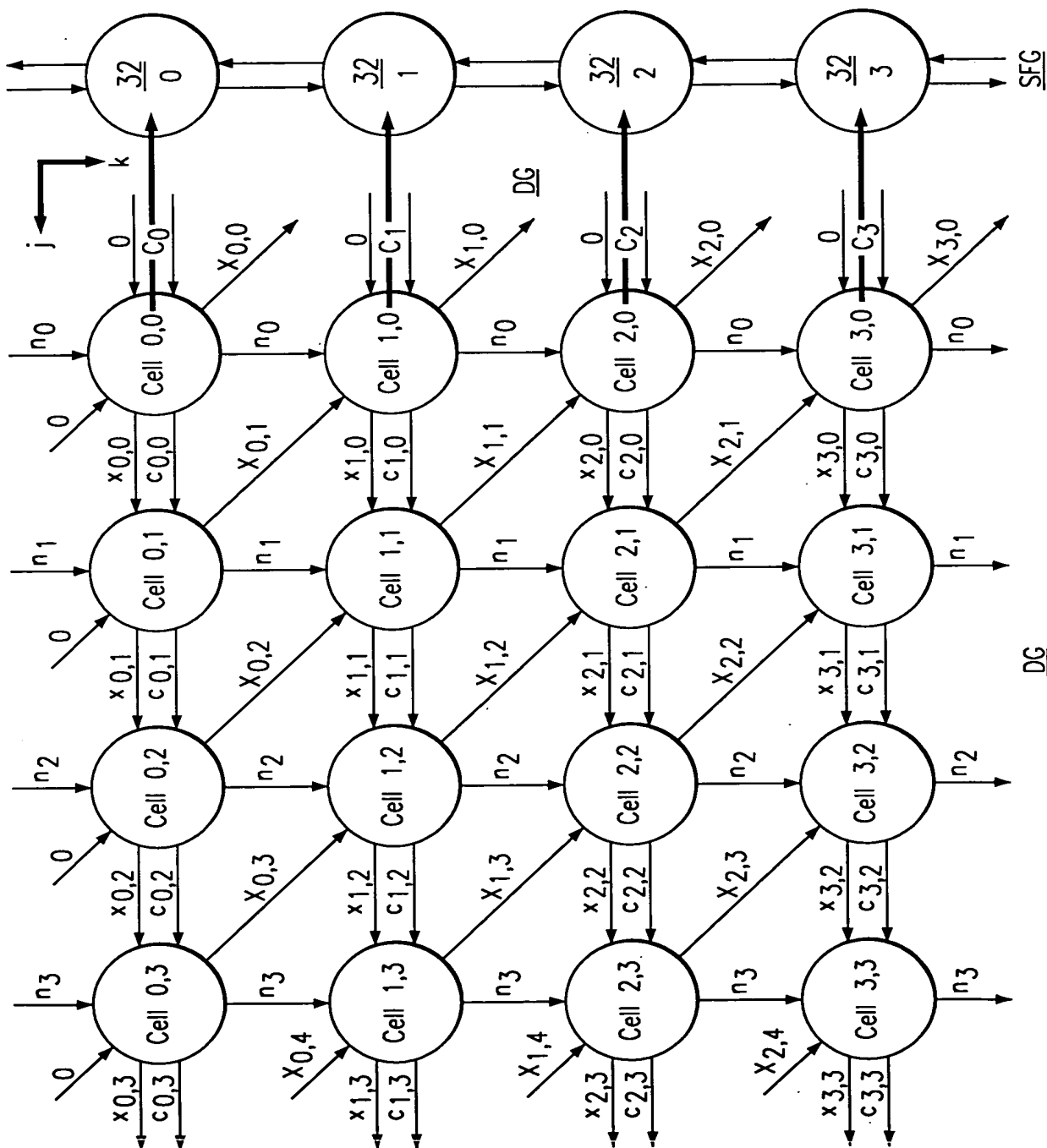


FIG. 17

FIG. 15



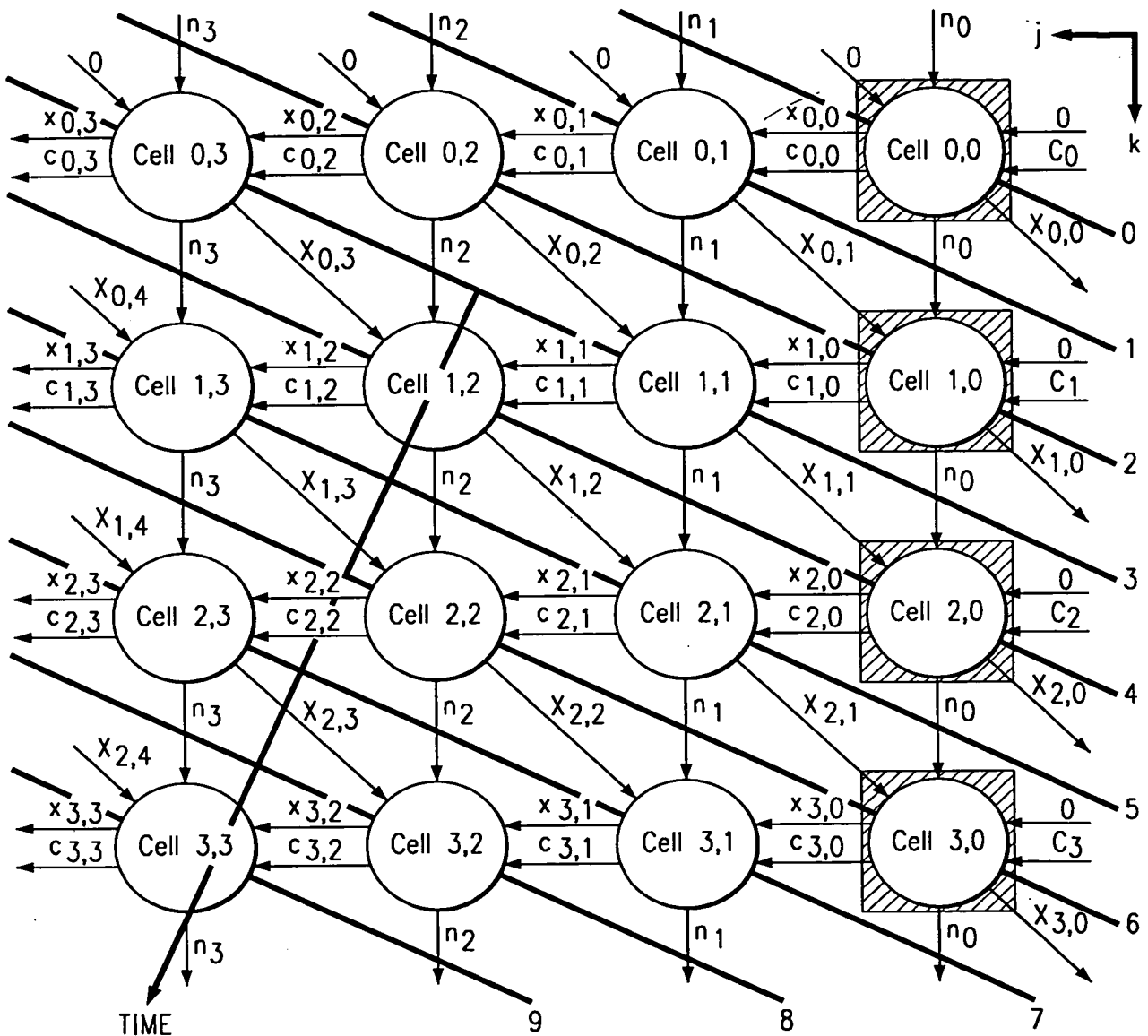
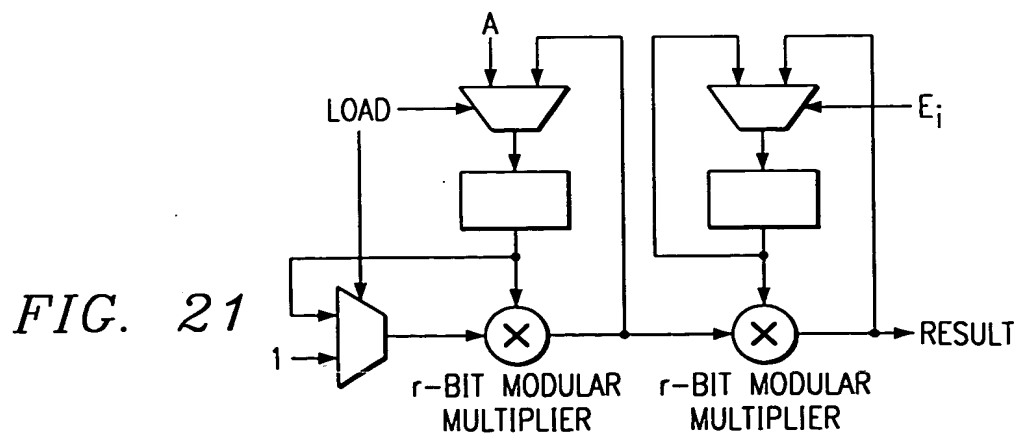
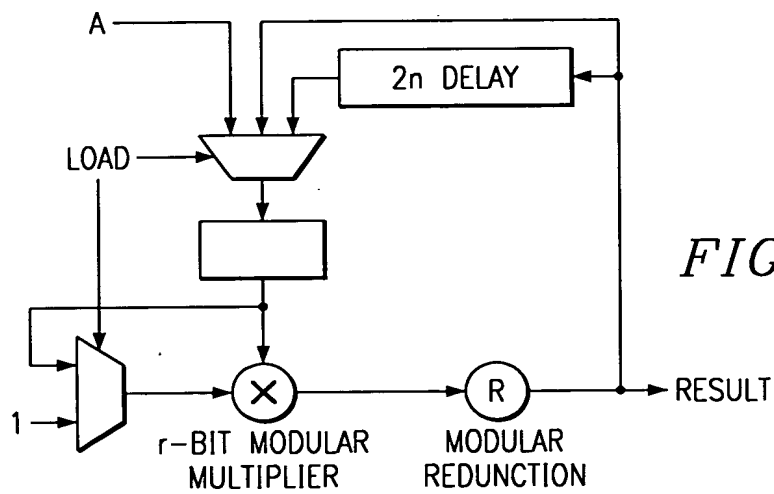
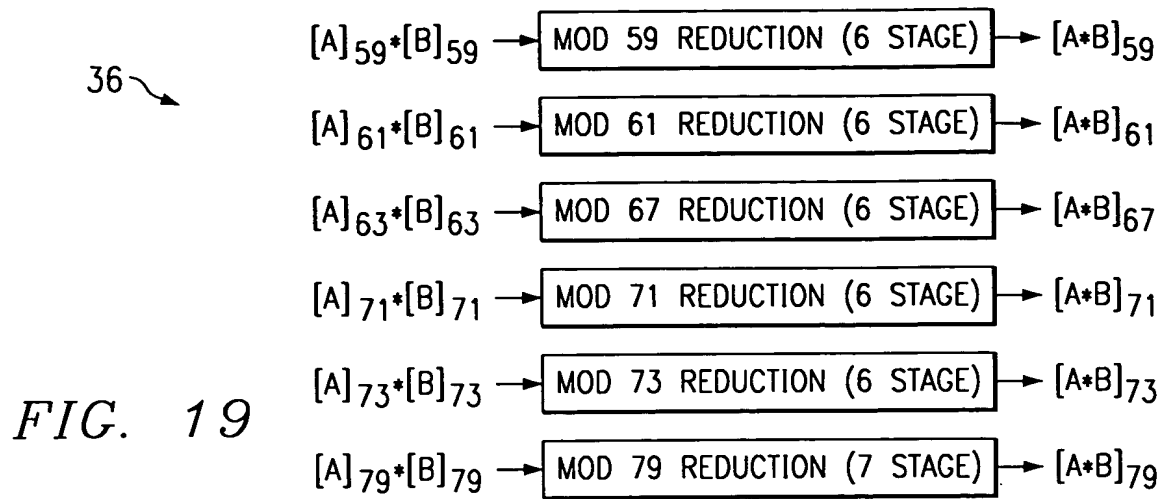
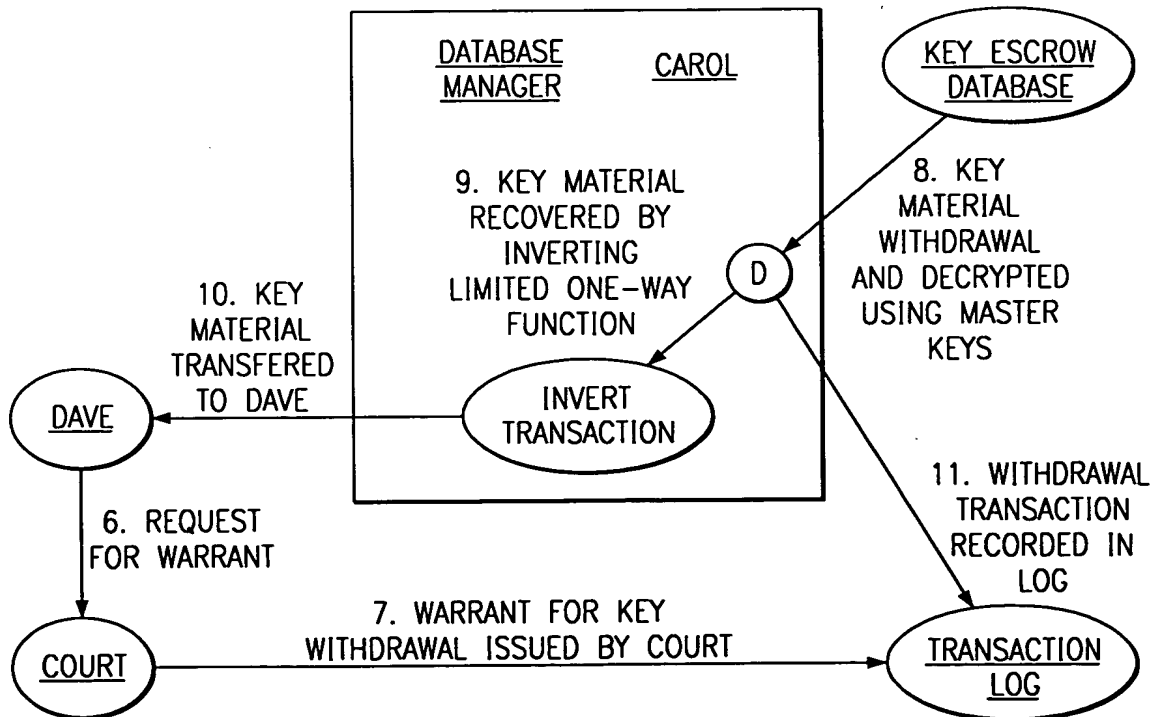
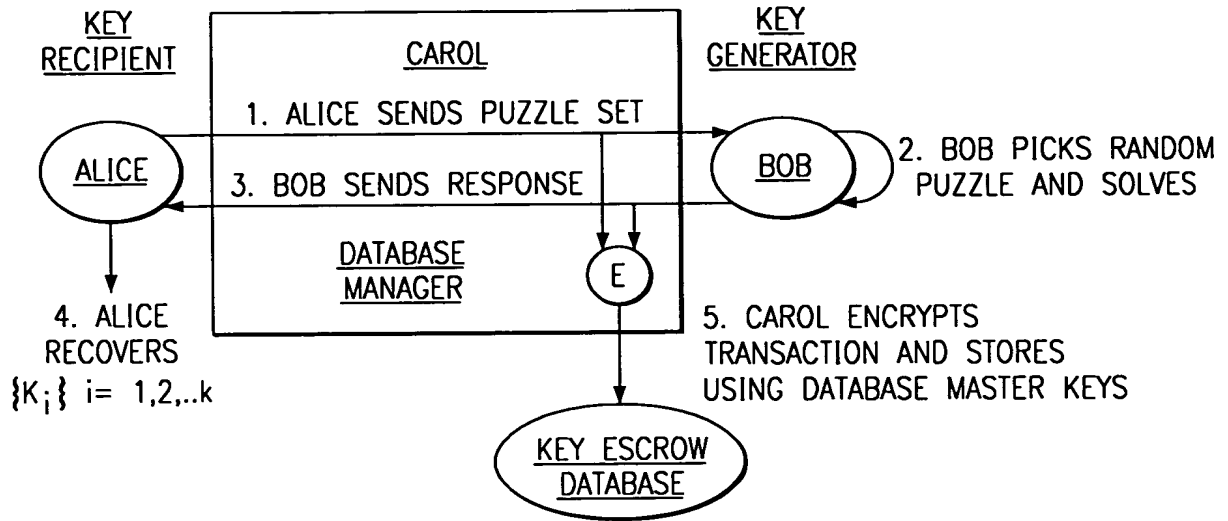


FIG. 16



The diagram illustrates a  $k$ -stage reduction pipeline. It starts with inputs  $A$  and  $B$  entering a multiplier ( $\times$ ). The output of the multiplier is loaded into a parallel load shift register. This register is connected to the  $A$  input of a full adder (FA) in the first stage of the pipeline. The carry-in (CI) of the FA is also loaded from a parallel load shift register. The output of the FA is connected to the  $S$  input of a carry adder (CA). The output of the CA is connected to the  $CO$  input of the next stage's FA. The final output  $Z$  is produced after  $k$  stages. The diagram also shows the internal structure of the pipeline, including the multiplier, full adder, and carry adder, and the flow of data through the stages.





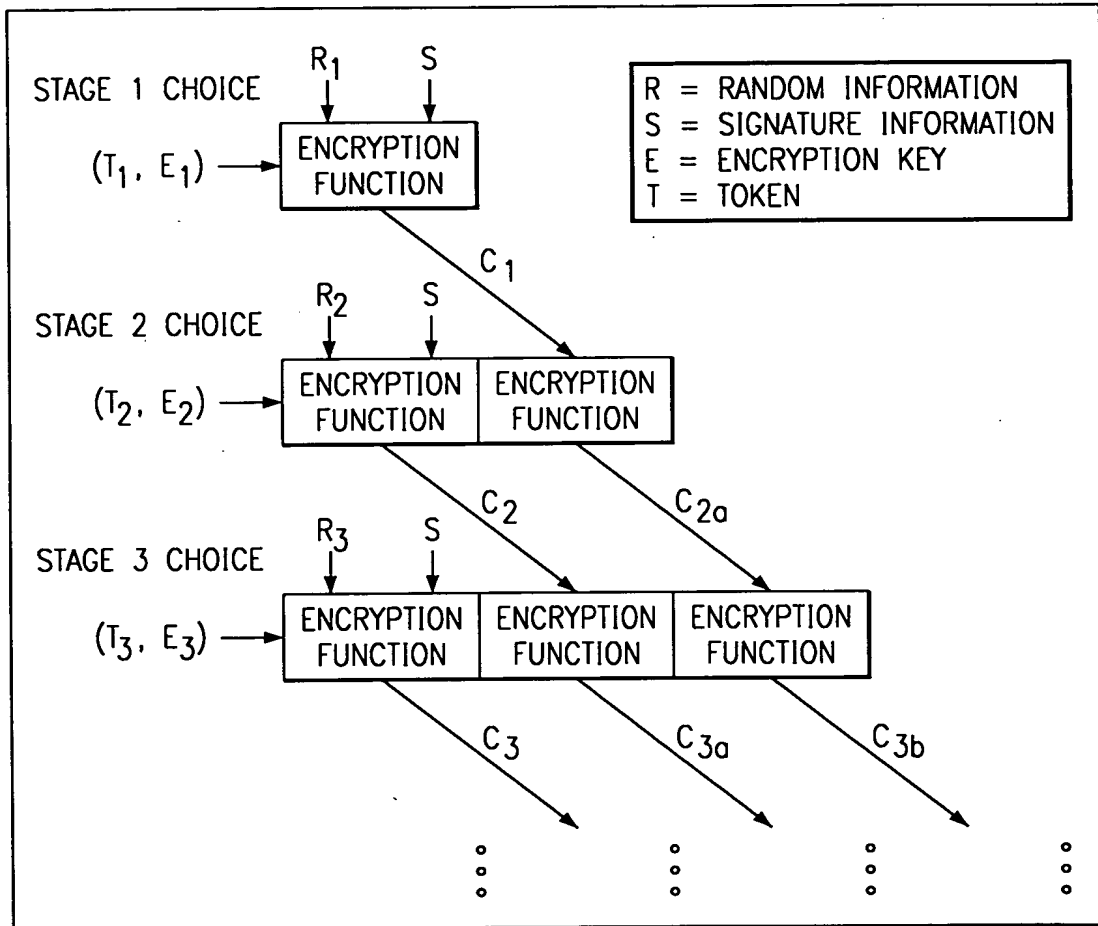


FIG. 26

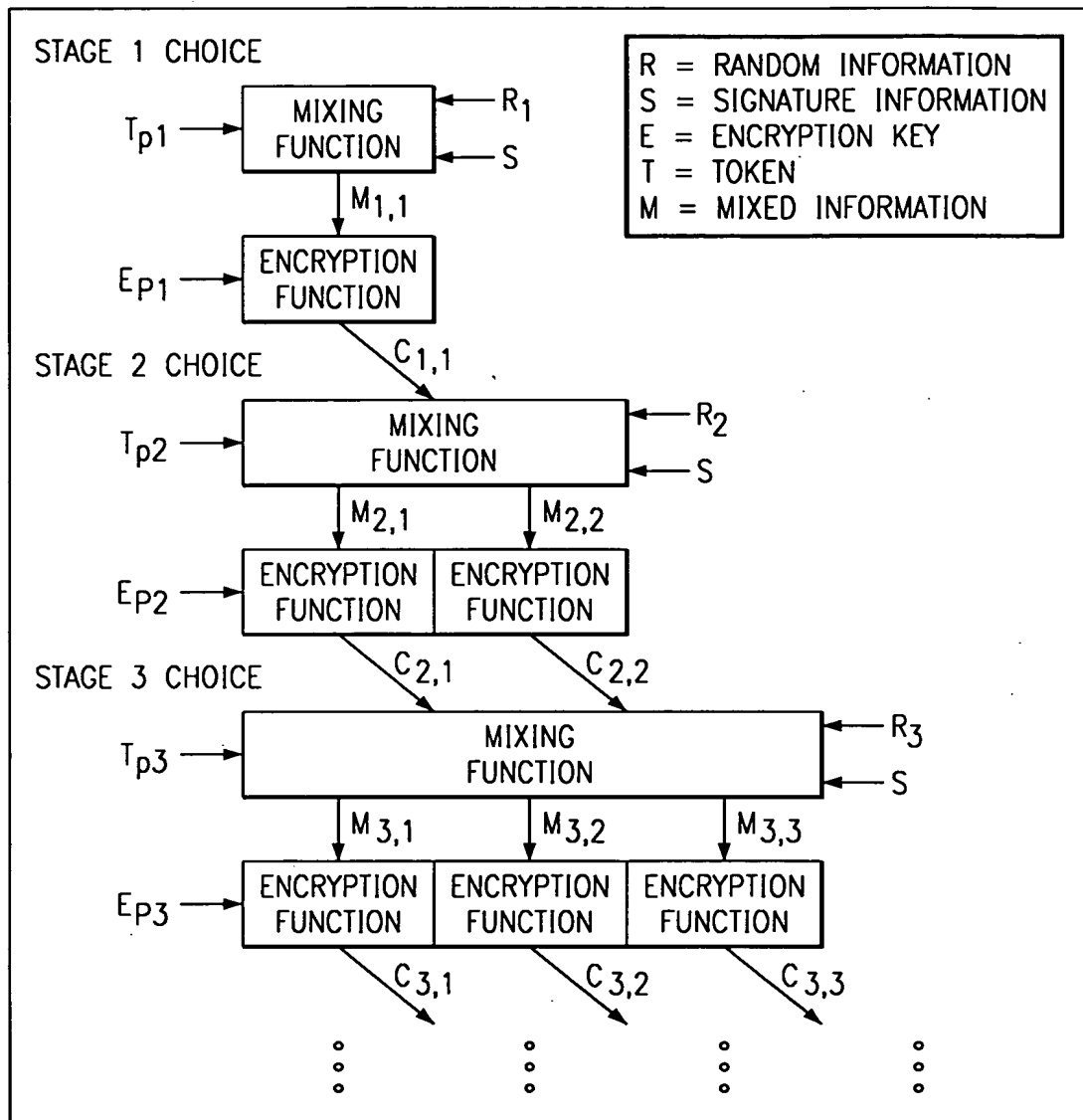


FIG. 27